

FIG. 1

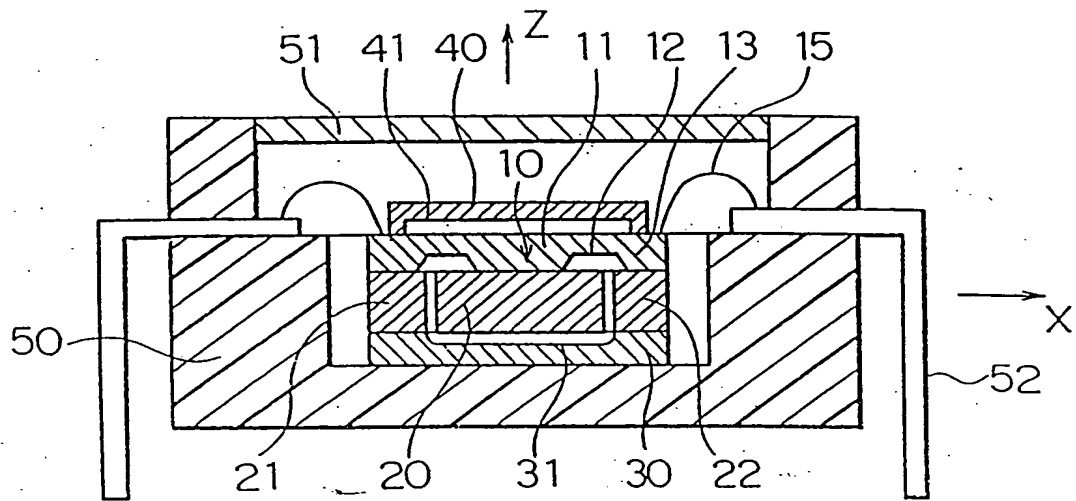


FIG. 2

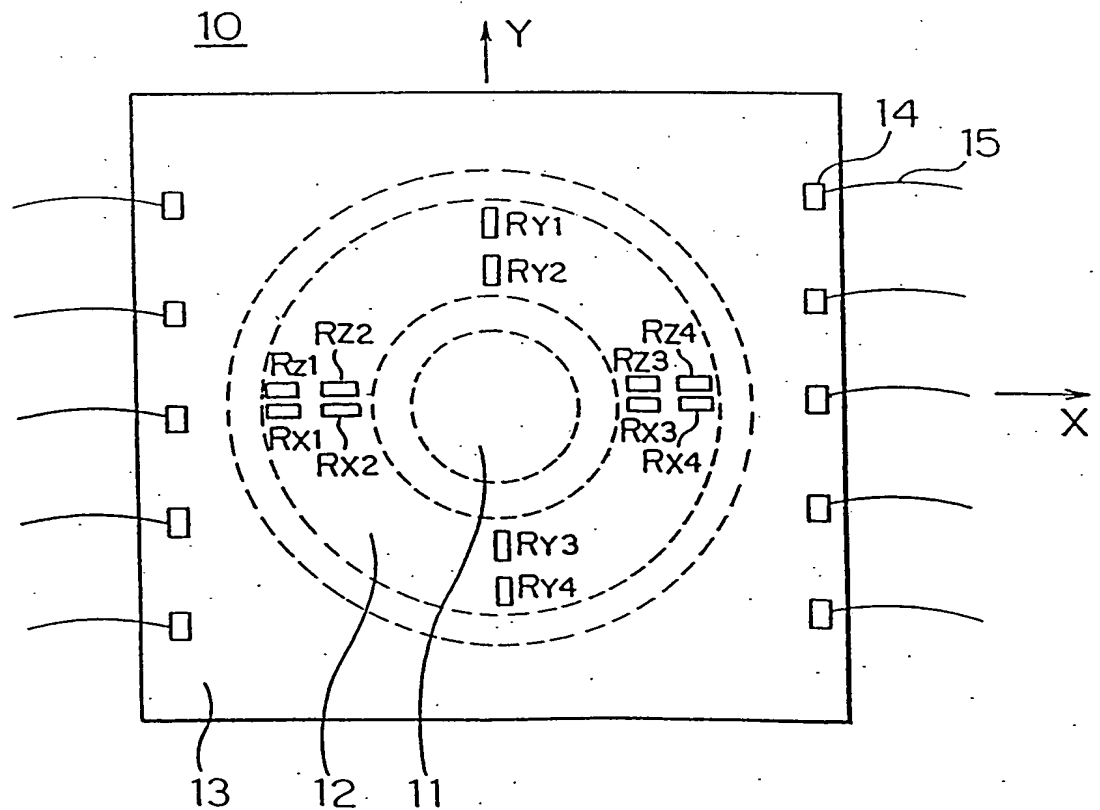


FIG. 3

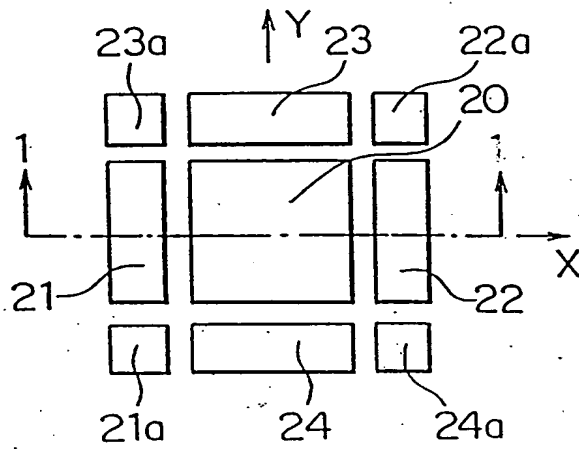


FIG. 4

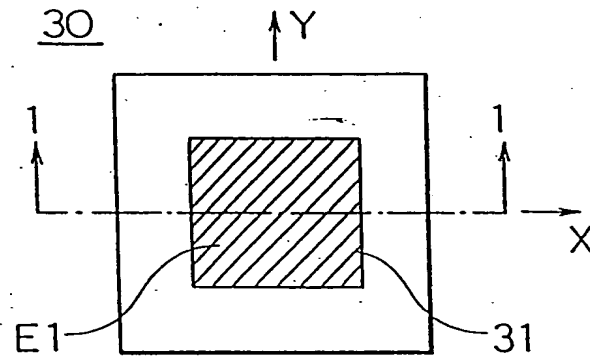


FIG. 5

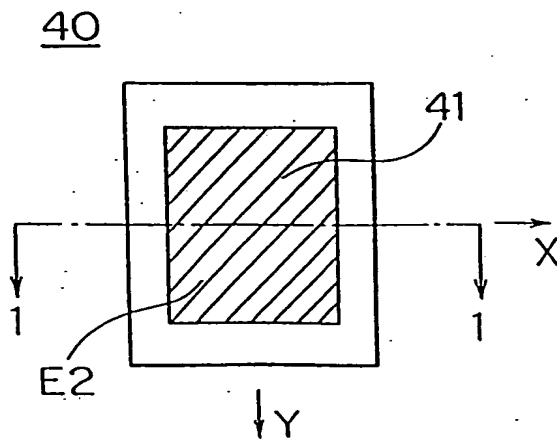


FIG. 6a

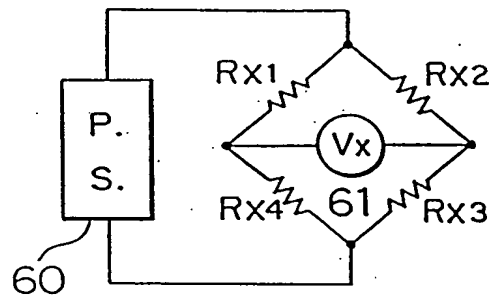


FIG. 6b

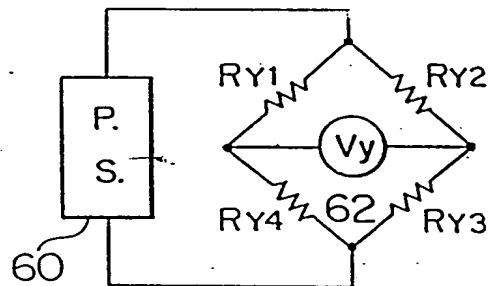


FIG. 6c

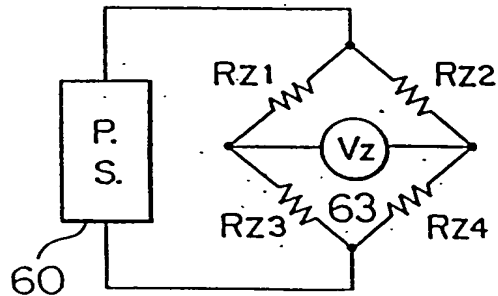


FIG. 7a

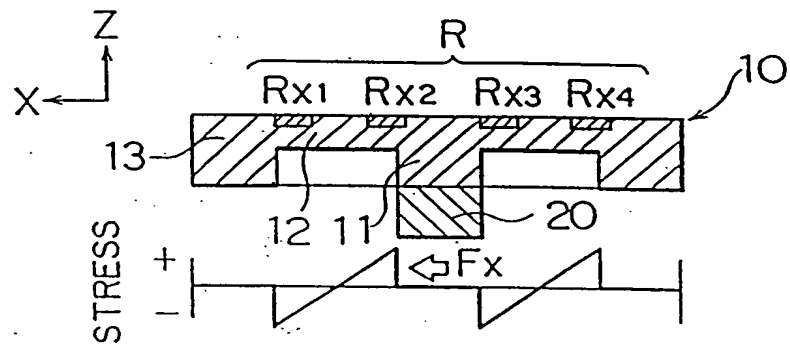


FIG. 7b

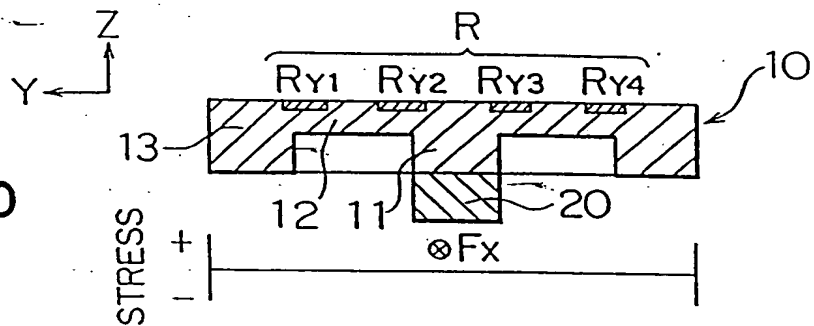
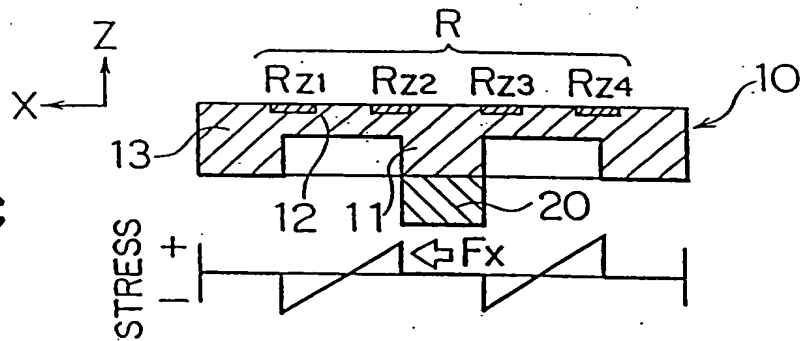
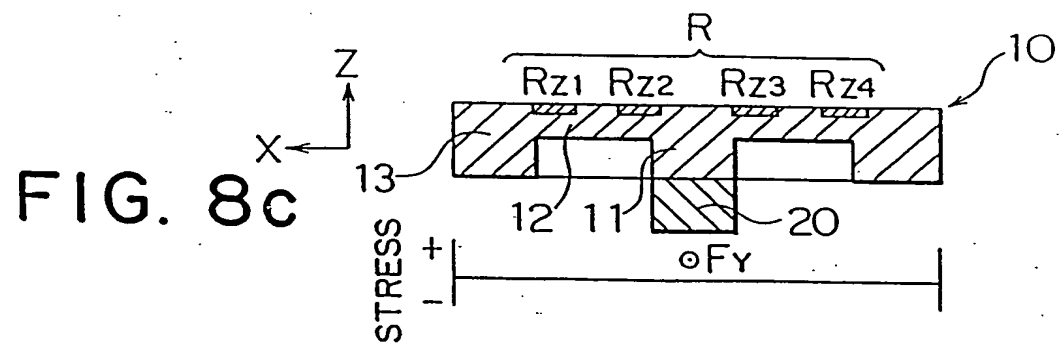
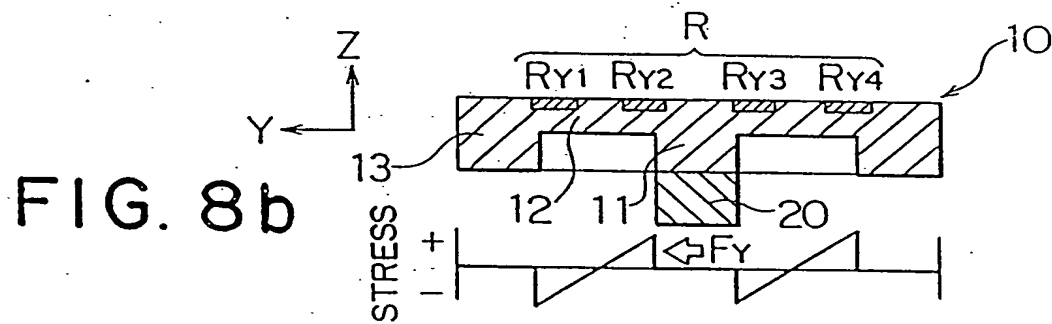
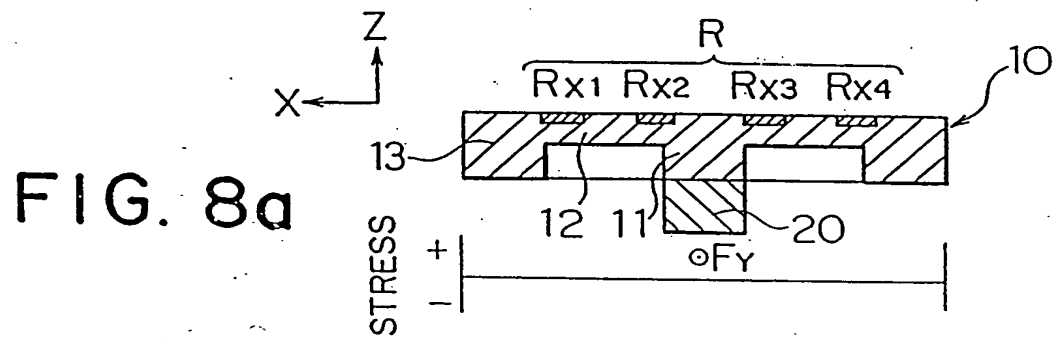
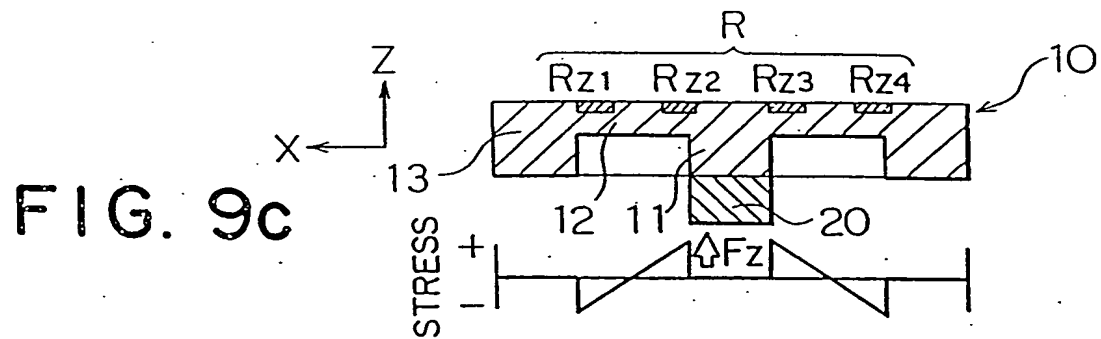
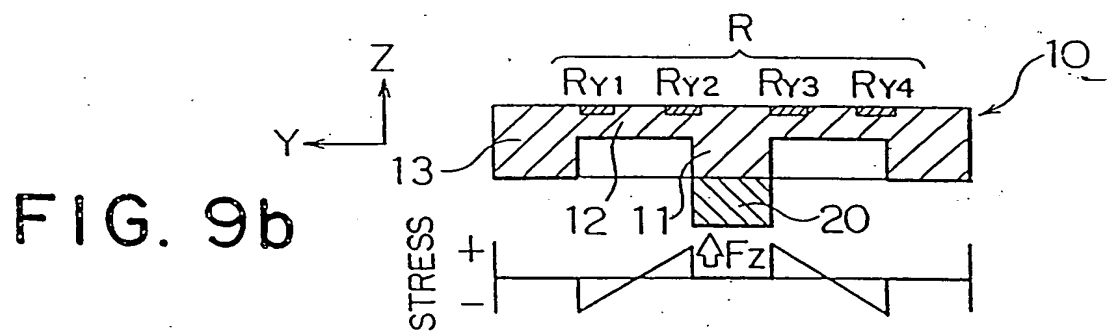
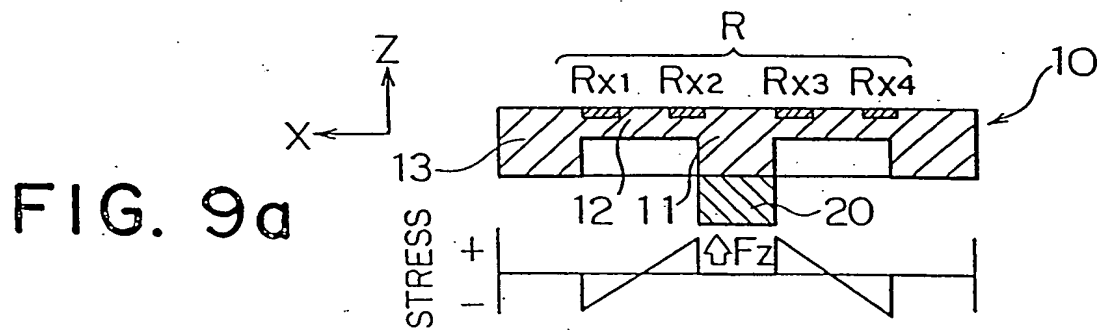


FIG. 7c







## FIG. 10

|                 | F <sub>x</sub> | F <sub>y</sub> | F <sub>z</sub> |
|-----------------|----------------|----------------|----------------|
| R <sub>x1</sub> | —              | 0              | —              |
| R <sub>x2</sub> | +              | 0              | +              |
| R <sub>x3</sub> | —              | 0              | +              |
| R <sub>x4</sub> | +              | 0              | —              |
| R <sub>y1</sub> | 0              | —              | —              |
| R <sub>y2</sub> | 0              | +              | +              |
| R <sub>y3</sub> | 0              | —              | +              |
| R <sub>y4</sub> | 0              | +              | —              |
| R <sub>z1</sub> | —              | 0              | —              |
| R <sub>z2</sub> | +              | 0              | +              |
| R <sub>z3</sub> | —              | 0              | +              |
| R <sub>z4</sub> | +              | 0              | —              |

FIG. 11

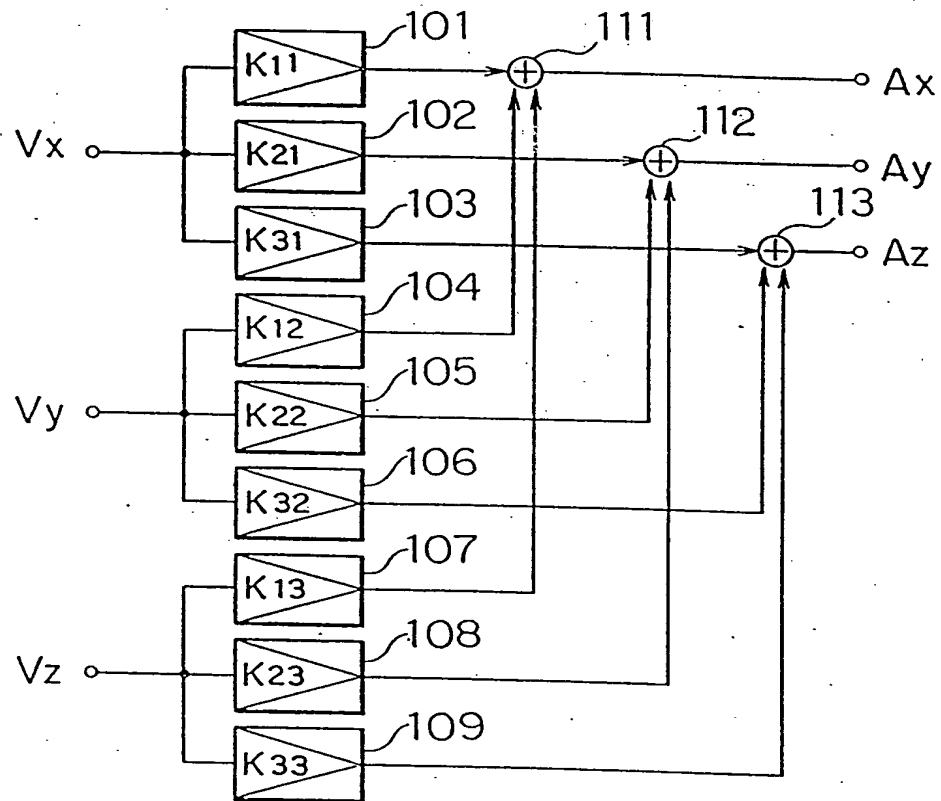


FIG. 12

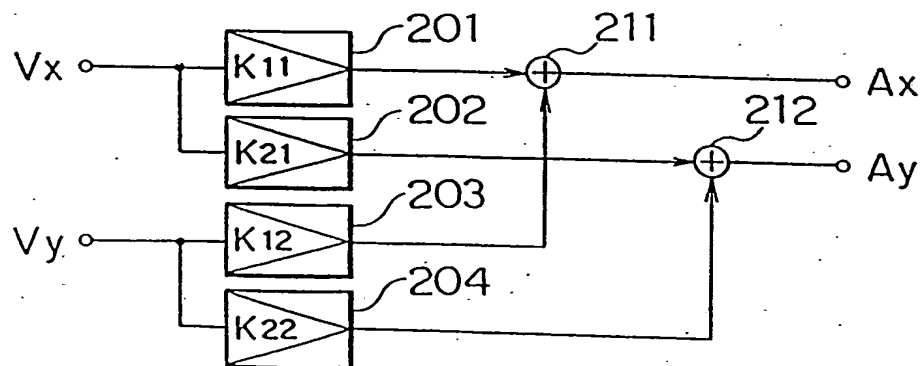




FIG. 13

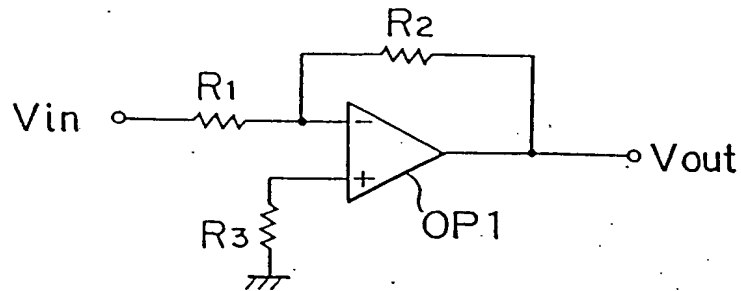


FIG. 14

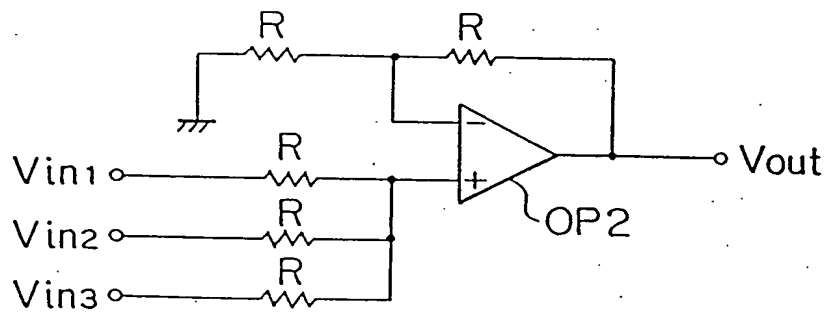


FIG. 15

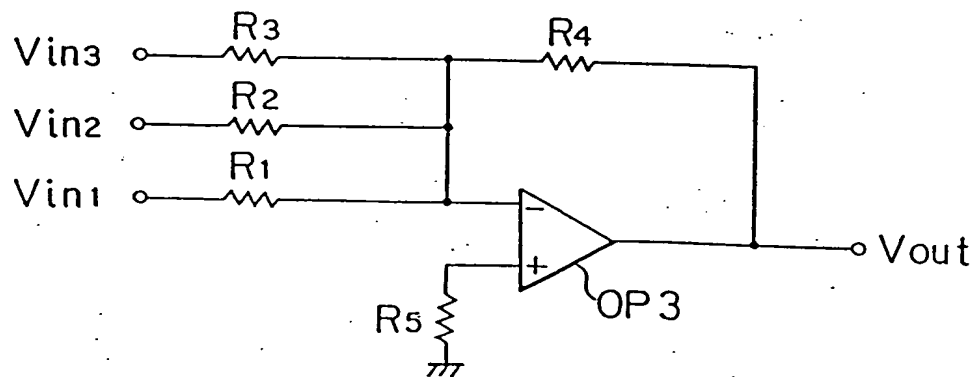


FIG. 16

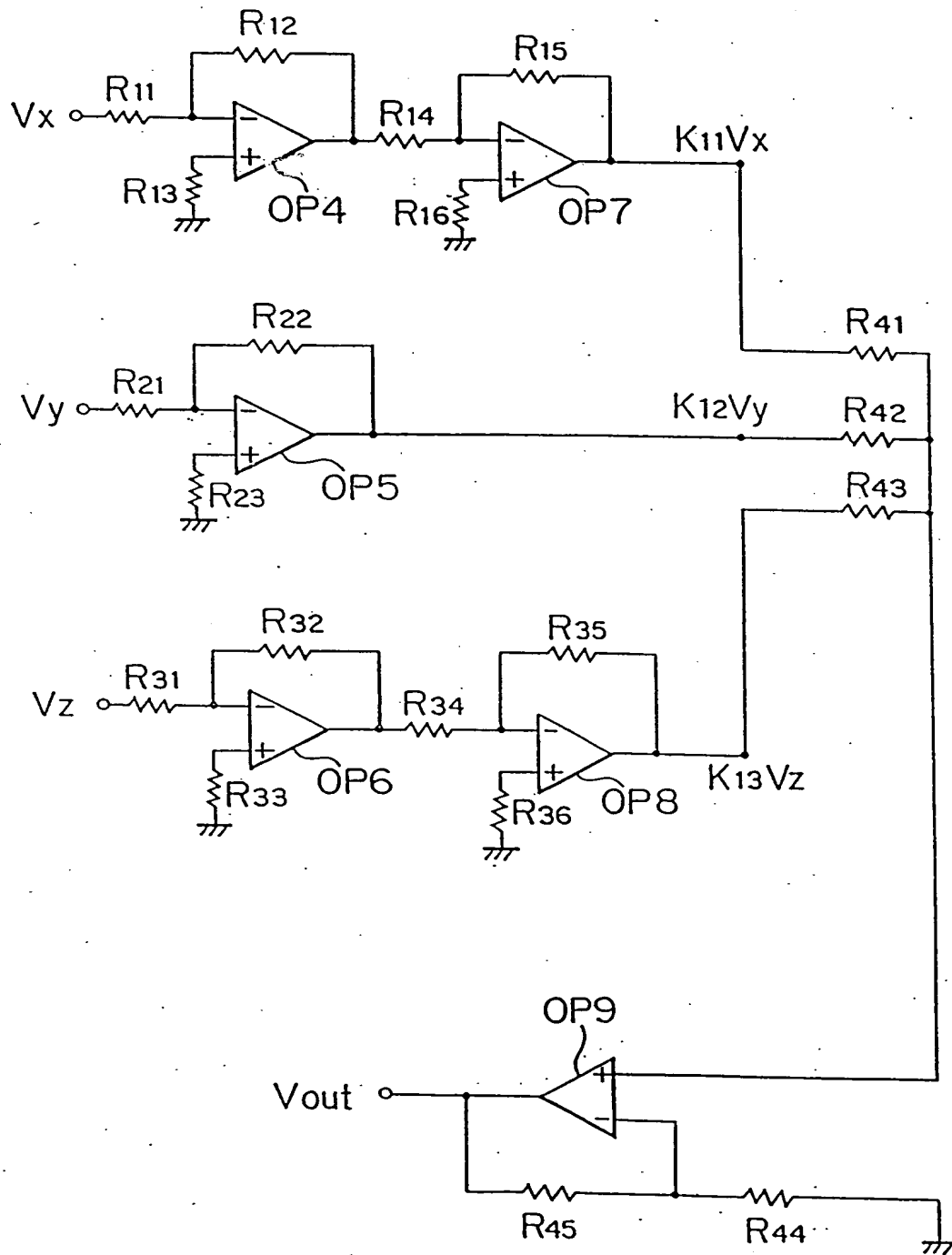


FIG. 17

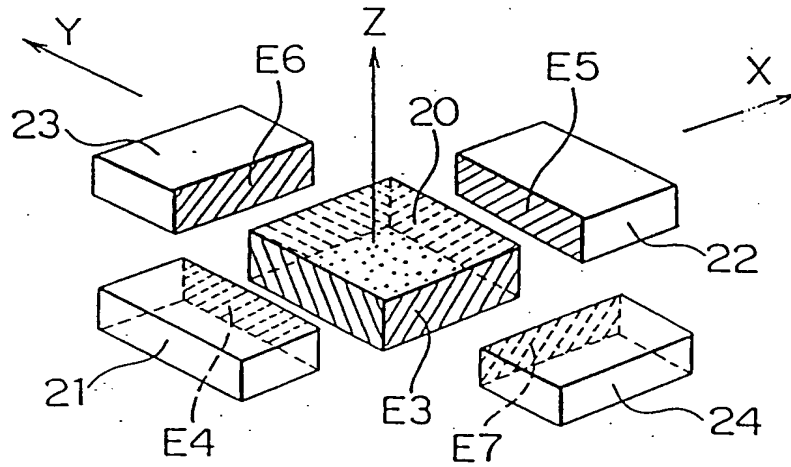


FIG. 18

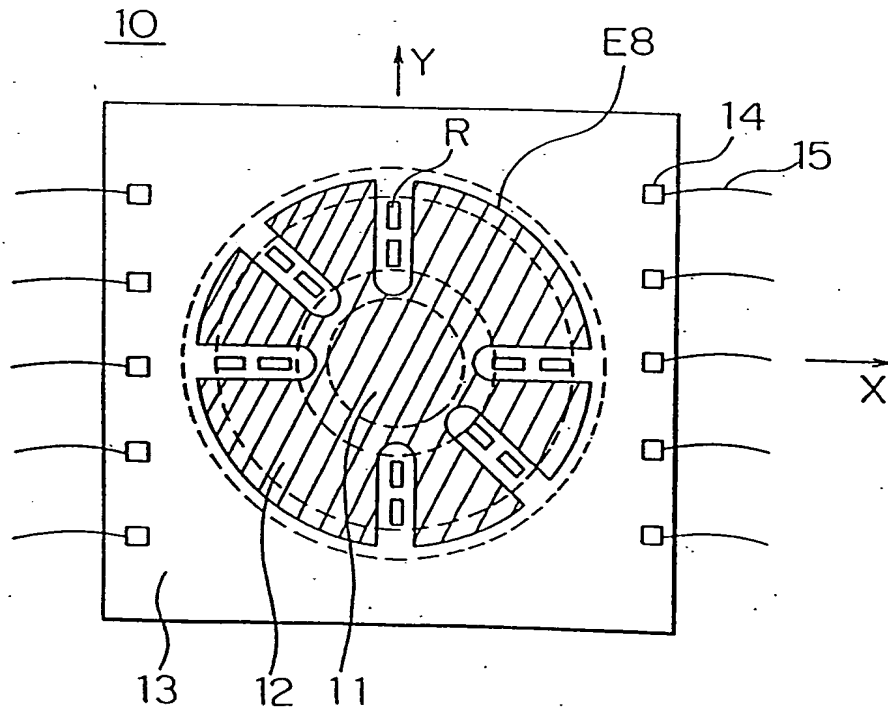


FIG. 19

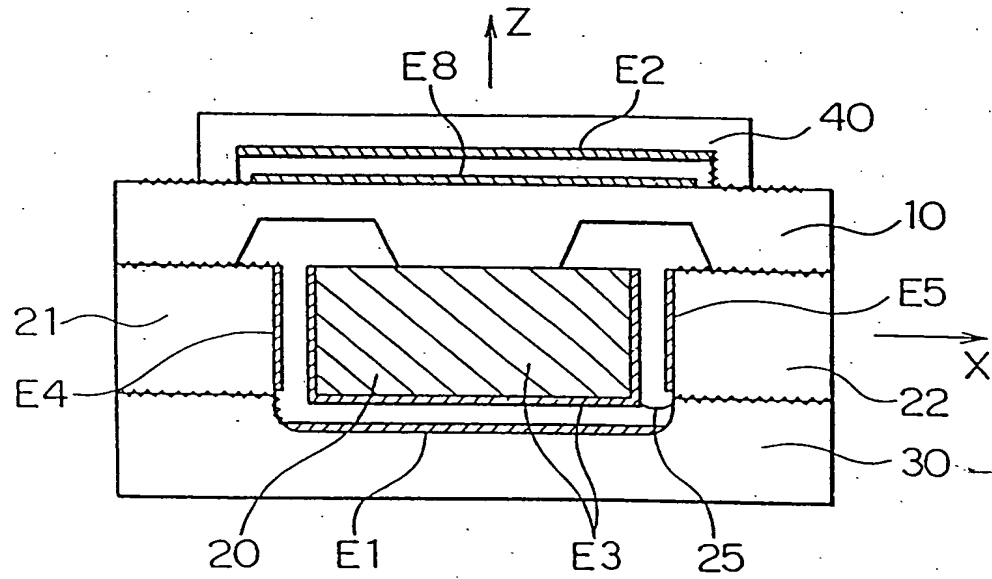


FIG. 20

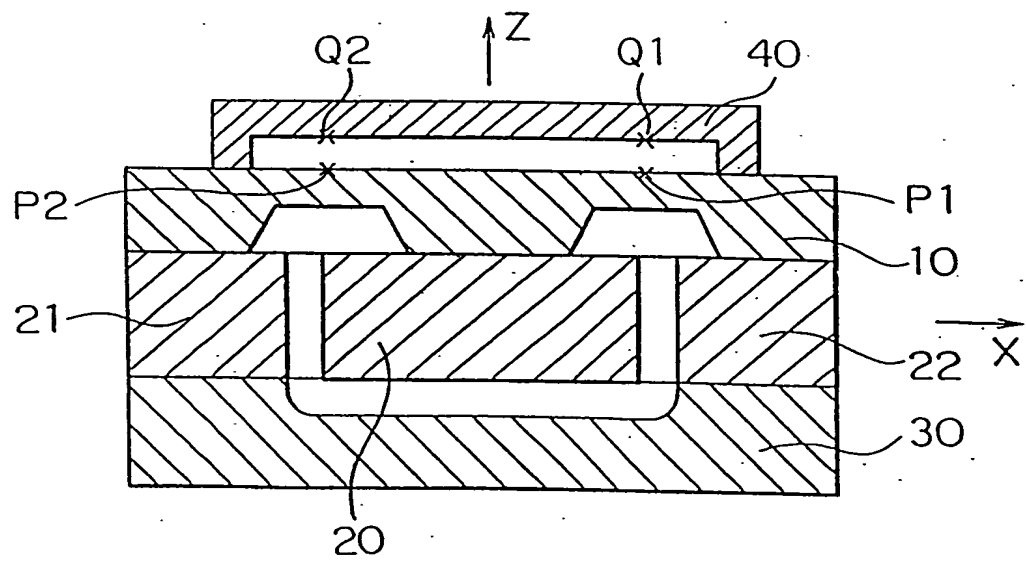


FIG. 21

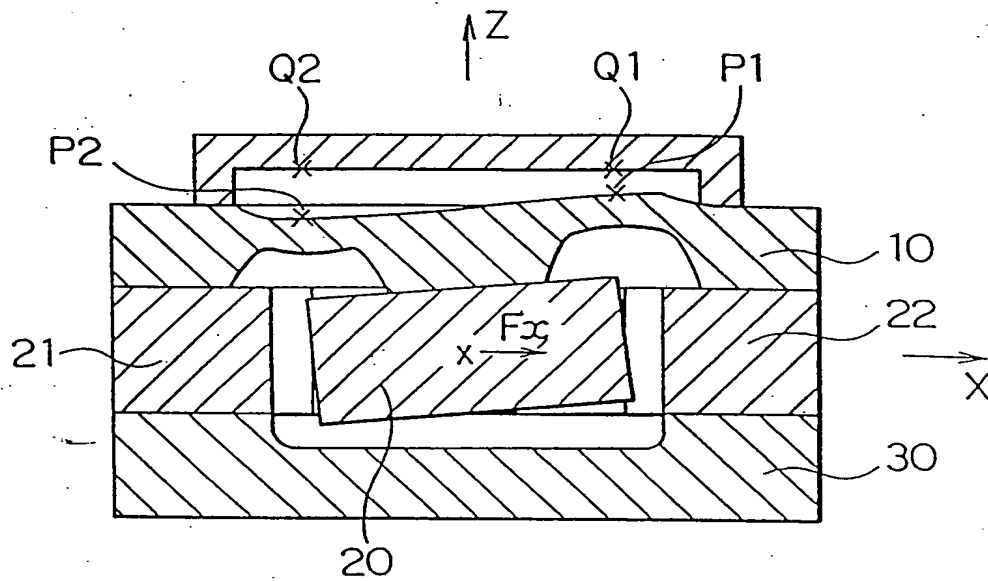


FIG. 22

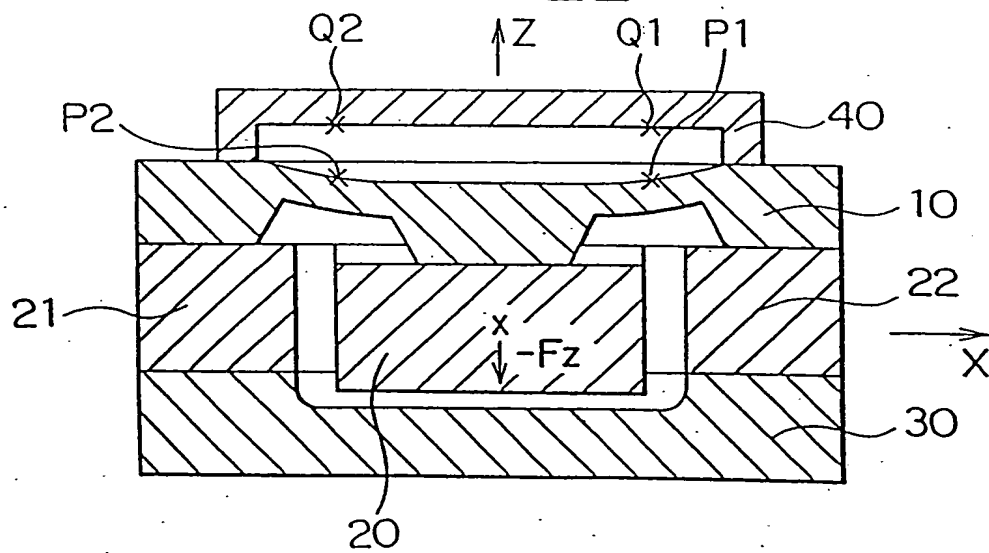




FIG. 25

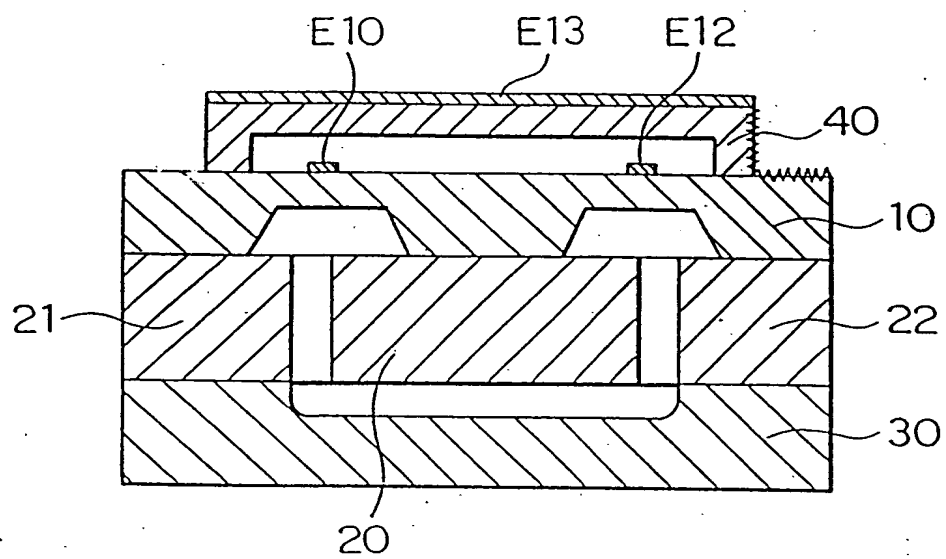


FIG. 26

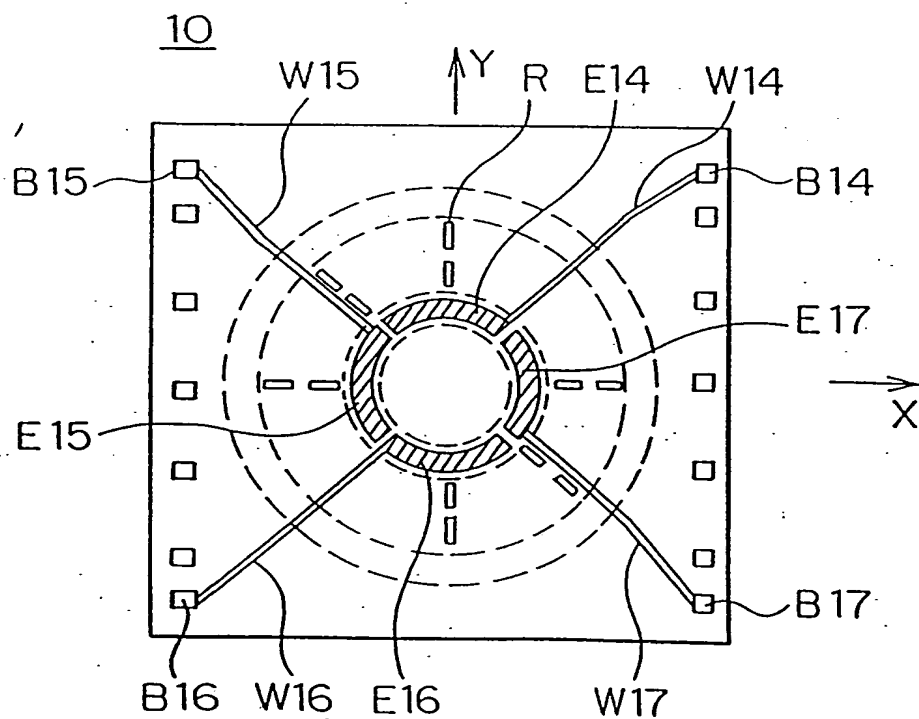


FIG. 27

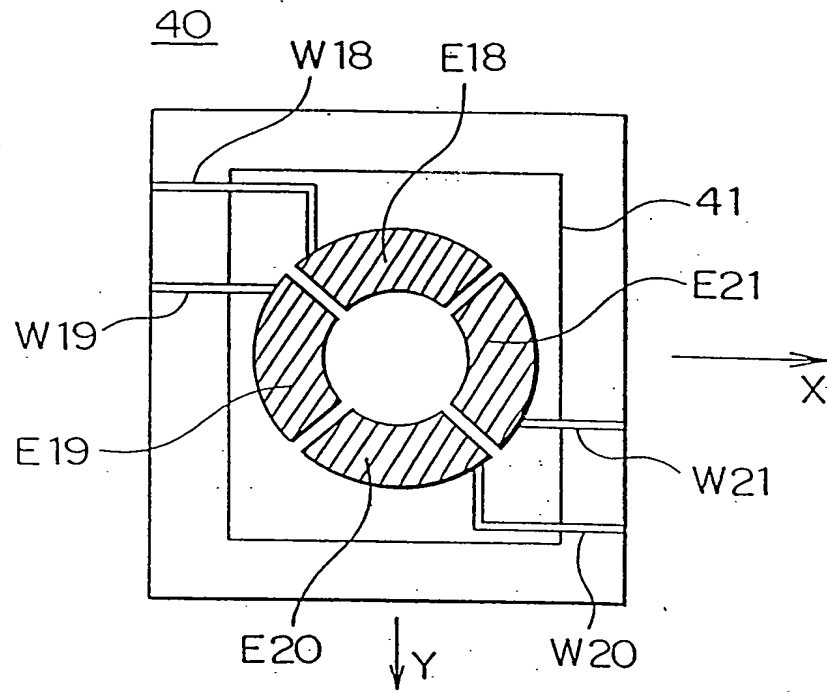


FIG. 28

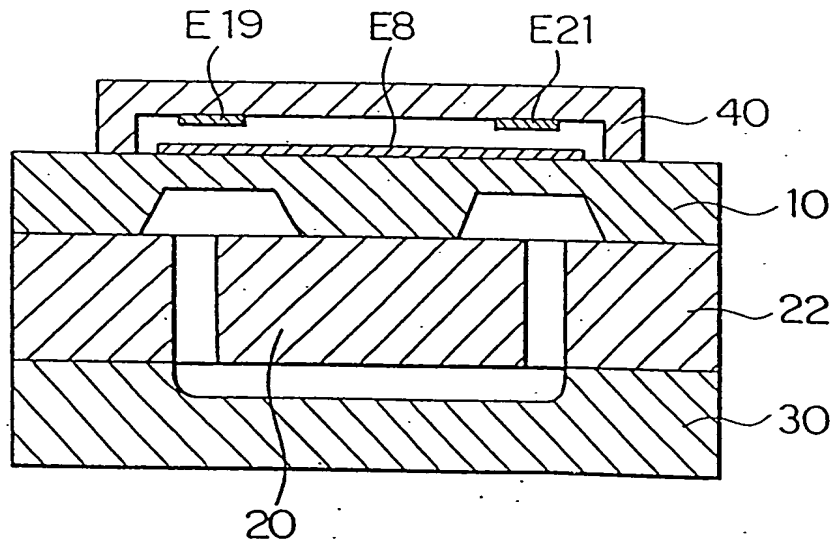




FIG. 29

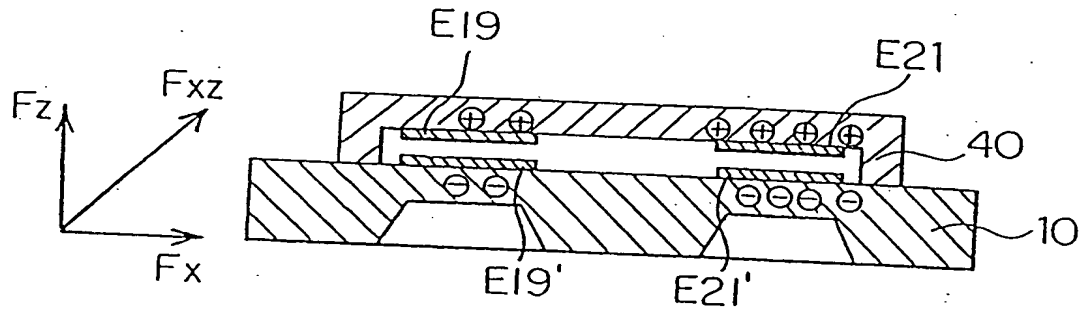


FIG. 30a

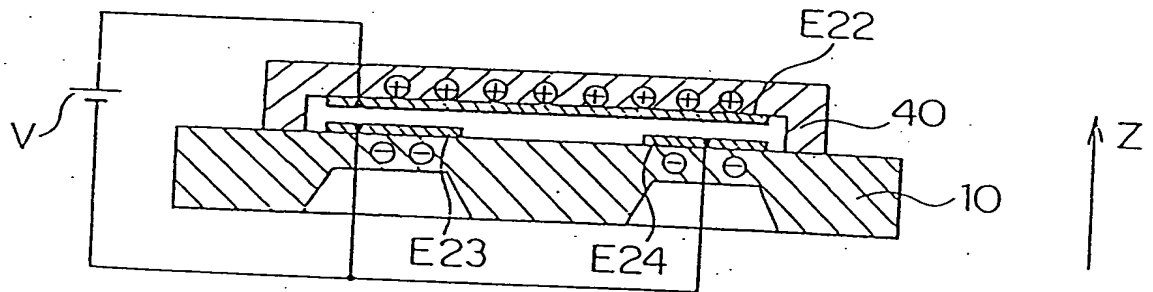
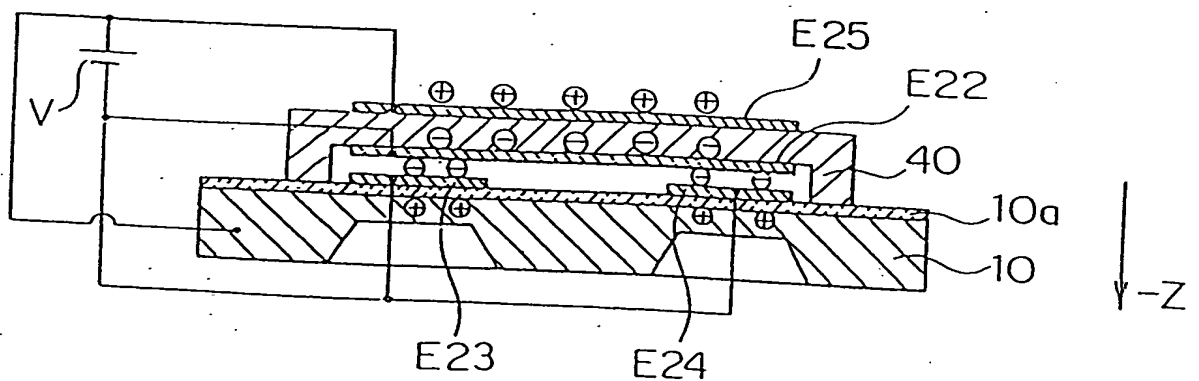


FIG. 30b



A cross-sectional view of a semiconductor device 300. The device is mounted on a substrate 420. A base layer 400 is formed on the substrate. A central region 310 contains a structure 311. This structure is surrounded by a layer 312. The entire central region is enclosed by a frame 313. The frame is supported by a base 330. The top of the device is covered by a layer 410. A layer 351 is formed on the top surface of the central region 310.

FIG. 33

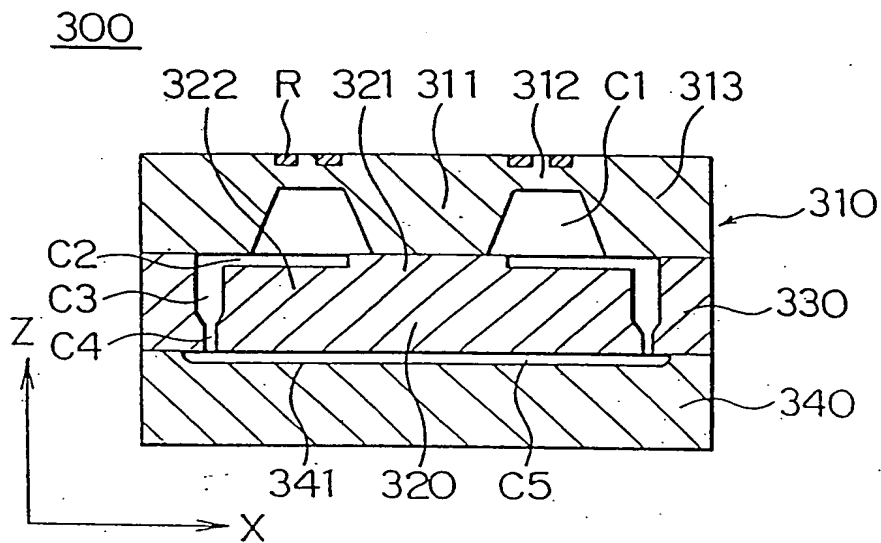
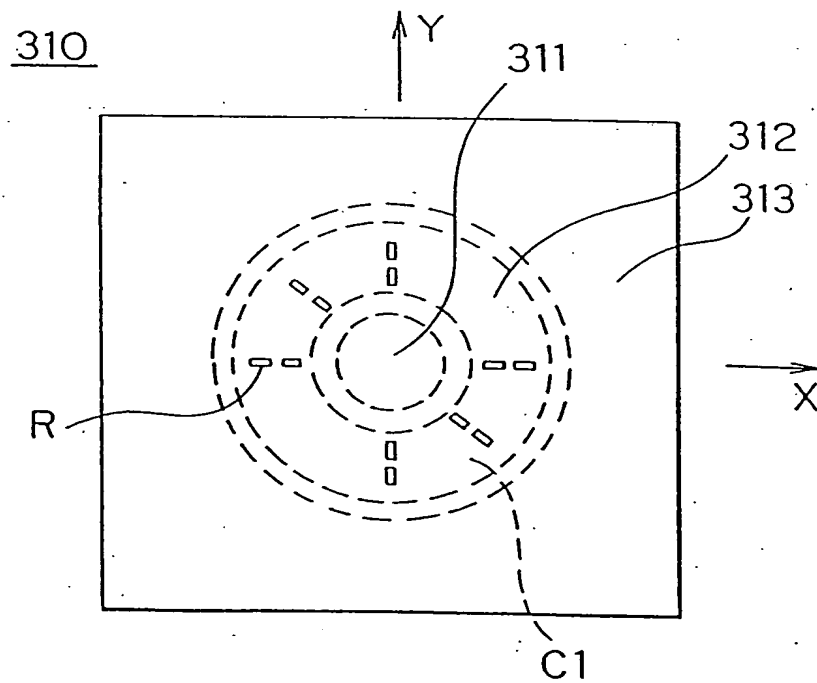


FIG. 34





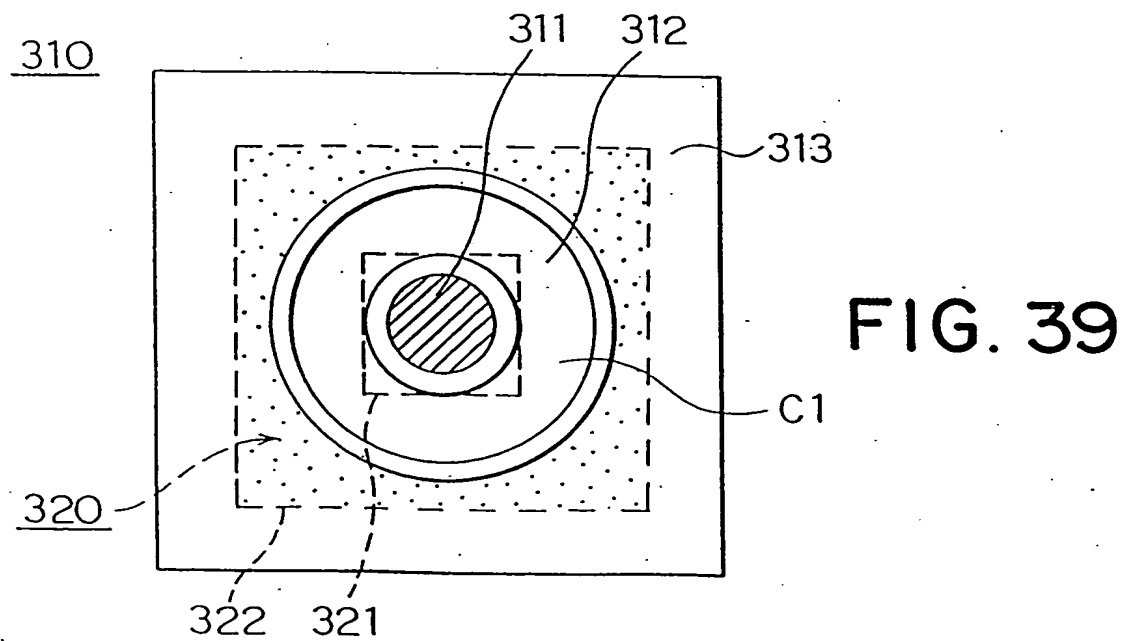
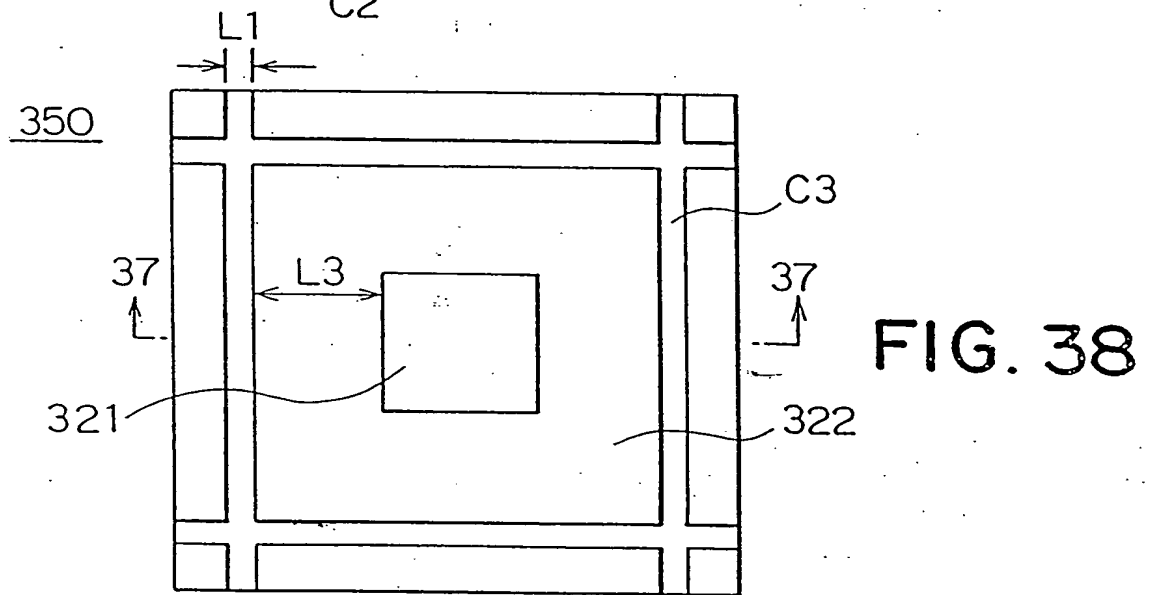
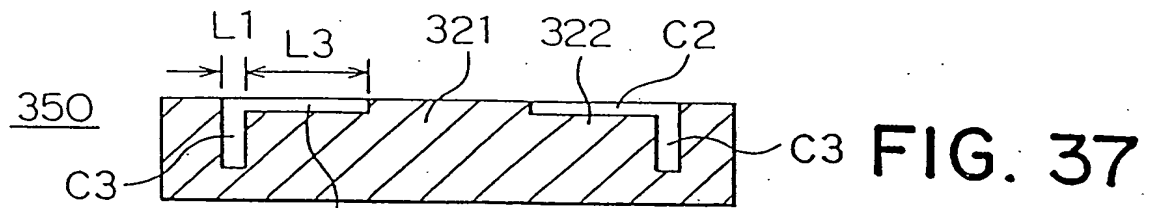


FIG. 40

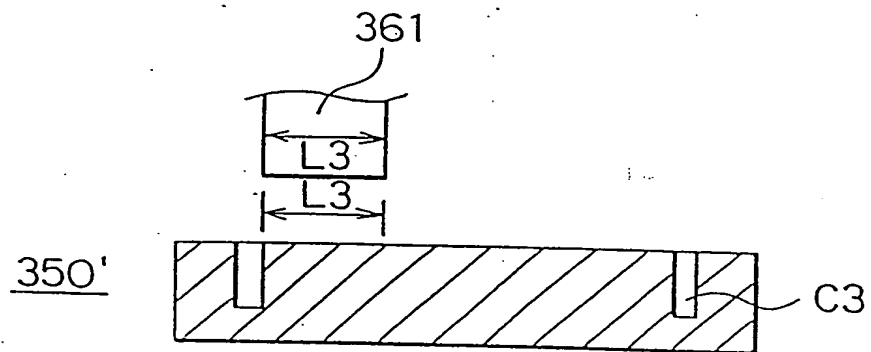
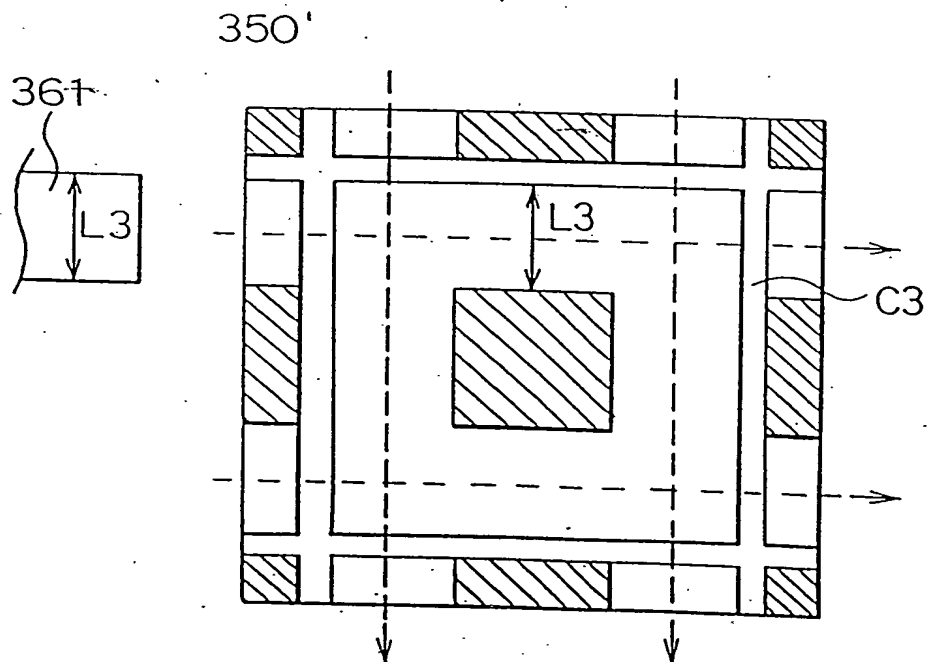


FIG. 41



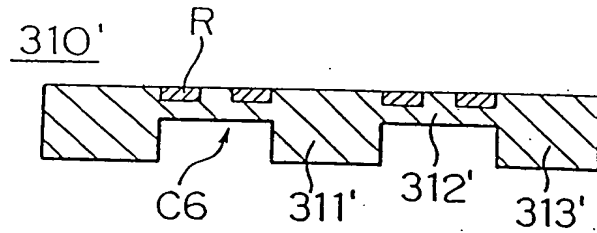


FIG. 42

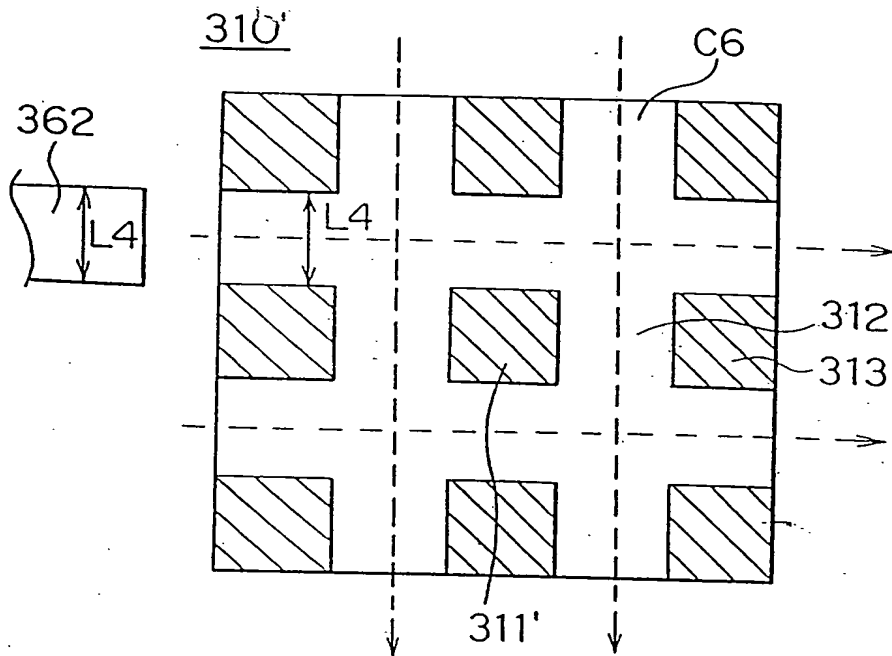


FIG. 43

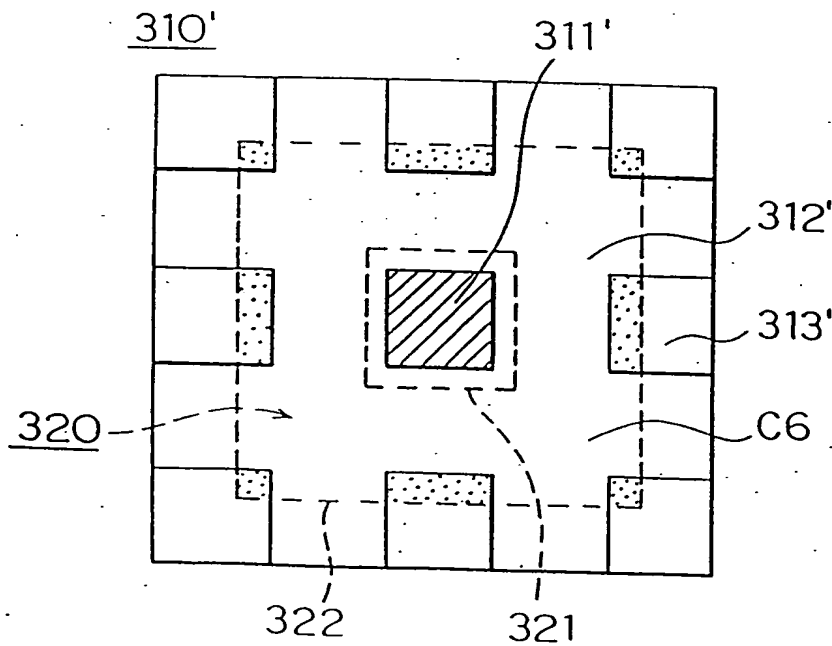


FIG. 44

FIG. 45

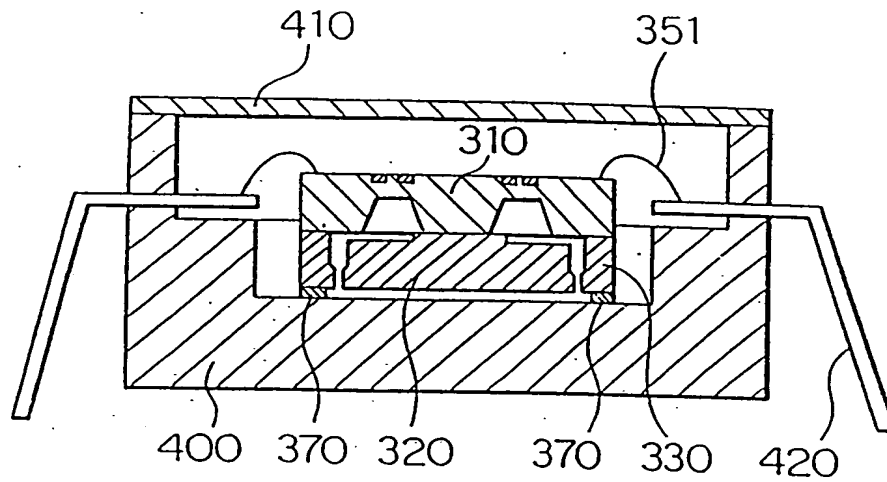


FIG. 46

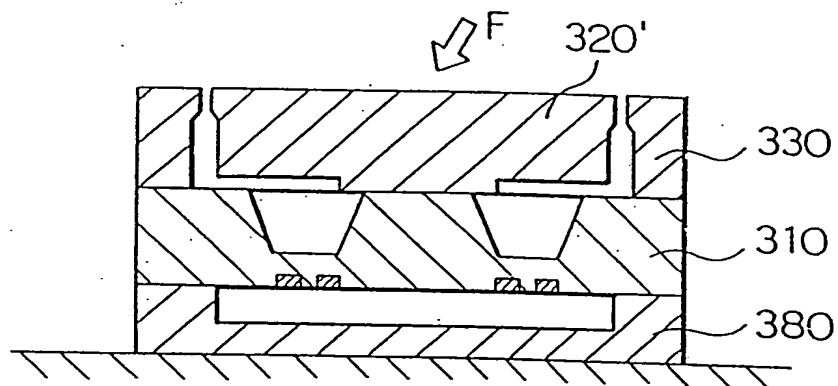


FIG. 47

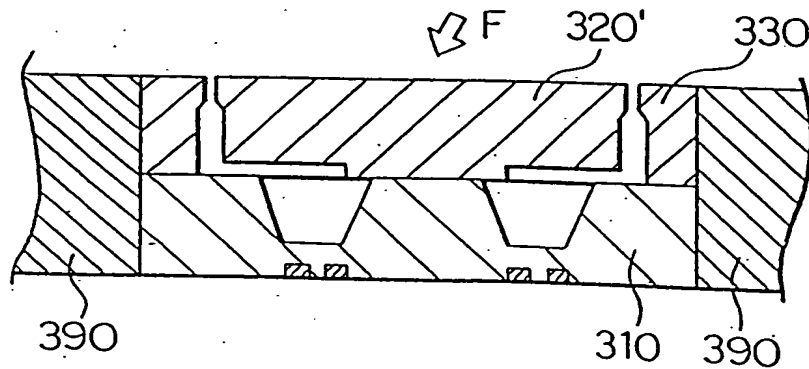




FIG. 48

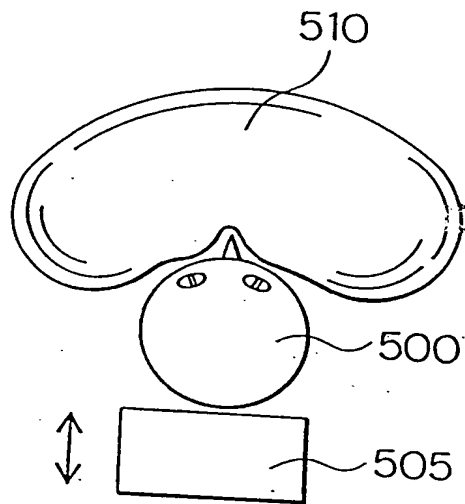


FIG. 49

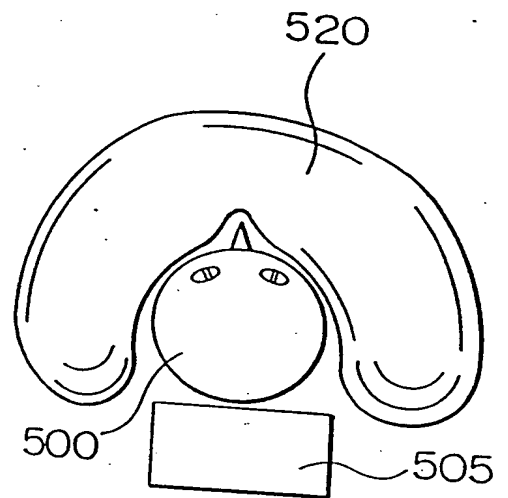


FIG. 50

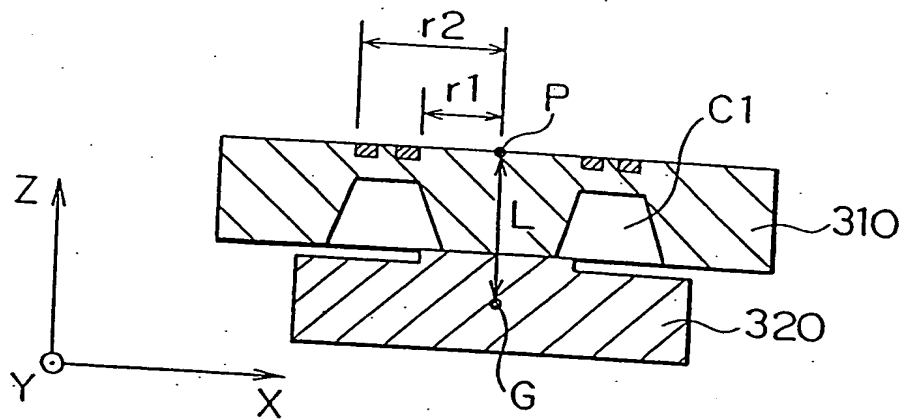


FIG. 51

300

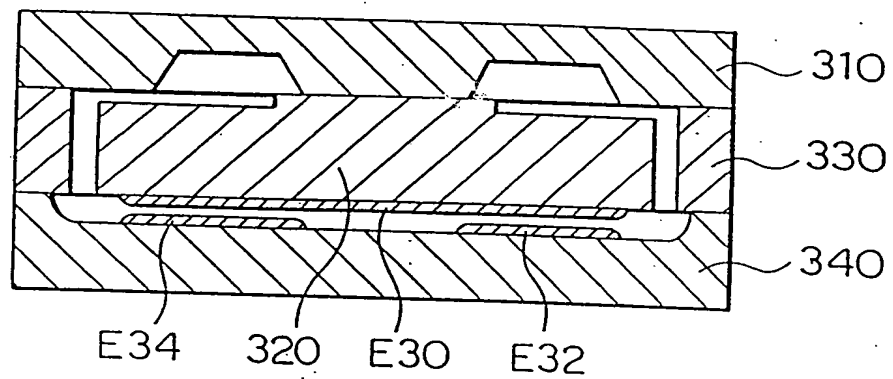


FIG. 52

340

